Gain drift compensation with no-feedback-loop developed for the X-IFU/Athena readout chain

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ABSTRACT

The focal plane of the X-ray Integral Field Unit (X-IFU) instrument of the Athena observatory is composed of about 4000 micro-calorimeters. These sensors, based on superconducting Transition Edge Sensors, are read out through a frequency multiplexer and a *base-band feedback* to linearize SQUIDs. However, the loop gain of this feedback is lower than 10 in the modulated TES signal bandwidth, which is not enough to fix the gain of the full readout chain. Calibration of the instrument is planned to be done at a time scale larger than a dozen minutes and the challenging energy resolution goal of 2.5 eV at 6 keV will probably require a gain stability larger than 10^{-4} over a long duration. A large part of this gain is provided by a Low-Noise Amplifier (LNA) in the Warm Front-End Electronics (WFEE). To reach such gain stability over more than a dozen minutes, this non-cooled amplifier has to cope with the temperature and supply voltage variations. Moreover, mainly for noise reasons, common large loop gain with feedback can not be used. We propose a new amplifier topology using diodes as loads of a differential amplifier to provide a fixed voltage gain, independent of the temperature and of the bias fluctuations. This amplifier is designed using a 350 nm SiGe BiCMOS technology and is part of an integrated circuit developed for the WFEE. Our simulations provide the expected gain drift and noise performances of such structure. Comparison with standard resistive loaded differential pair clearly shows the advantages of the proposed amplifier topology with a gain drift decreasing by more than an order of magnitude. Performances of this diode loaded amplifier are discussed in the context of the X-IFU requirements.

Keywords: Gain drift compensation, Low Noise Amplifier, Optimum Noise, X-ray detectors readout electronics, Transconductance, Shot noise, Bipolar technology

1. INTRODUCTION

The Advanced Telescope for High-ENergy Astrophysics (ATHENA[1]) is an ESA L-class space mission dedicated to the topic of "The Hot and Energetic Universe" that foresees the launch of a large X-ray astronomy observatory in 2028. The primary science objectives of the mission are the study of the cosmic large-scale structures and in particular of the hot gas of the galaxy clusters and the study of the growth and evolution of the super-massive black holes of the universe. The ATHENA satellite will carry a 12 m long X-ray mirror telescope with a large effective area of 2 m^2 (at 1 keV) and two instruments that will alternatively be at the telescope focal plane: a Wide Field Imager (WFI) for deep and large field-of-view X-ray imaging and an X-ray Integral Field Unit (X-IFU) for very high spectral resolution imaging. This paper discusses the development of a component of the X-IFU instrument. The X-IFU[2] is based on about 4000 Transition Edge Sensors (TES) micro-calorimeter cooled down to 50 mK and read out by two stages of Supeconducting QUantum Interference Devices (SQUID) trans-impedance amplifiers. Each TES is associated with its own LC filter to select one of the carrier frequencies. So, a frequency domain multiplexing is performed by modulating TES with 40 separate carriers between 1 MHz to 6 MHz. This reduces by a factor of 40 the number of wires needed to read out the full focal plane. After the SQUID stages, a Warm Front End Electronics (WFEE), operating at room temperature, further amplifies the signal minimizing the additional noise (Low Noise Amplifier, LNA), just before digitization by an Analog to Digital Converter (ADC) and further processing by the Digital Readout Electronics (DRE[3]). Figure 1 shows

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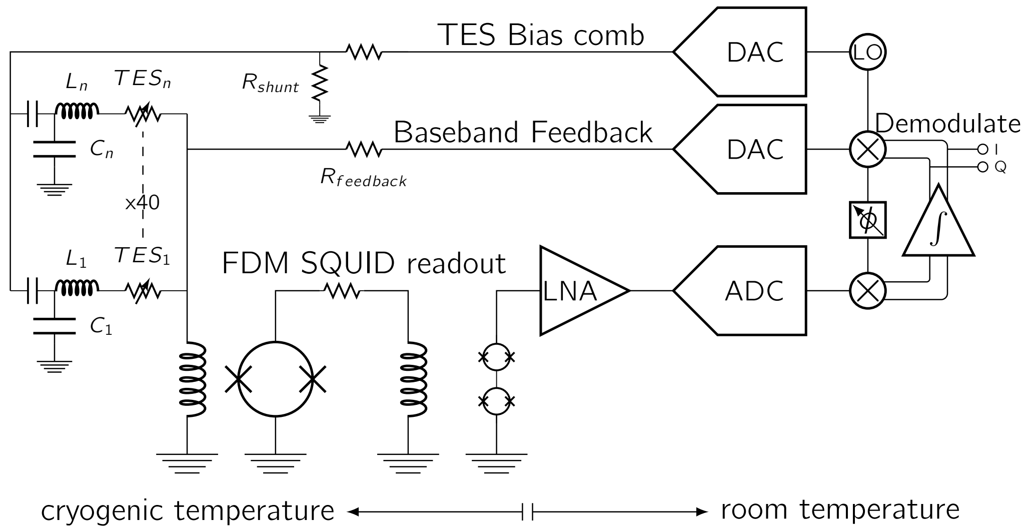

Figure 1. A simplified schematic of the Athena X-IFU TES readout. The LNA, part of this readout chain, amplifies the signal to match the ADC dynamic range. Frequency domain multiplexing (FDM) is obtained by modulating each TES with one of the "Bias comb" carriers. Base-band feedback relaxes the dynamic requirement of the readout chain by suppressing the carriers from the modulated TES signals amplified by SQUID and LNA.

a simplified schematic of the TES multiplexed readout and the base-band feedback developed for the X-IFU instrument.

The LNA is a key element of the WFEE that provides the amplification of the signal for an efficient low noise digitization by ADC. Moreover, long-term stability of the LNA voltage gain is required to guaranty the unprecedented energy resolution of the X-IFU instrument. Indeed, mainly for crosstalk reasons, the loop gain of the base-band feedback can not be large enough to fix the gain of the whole readout chain and is essentially used to nullify the FDM carriers. In this paper we discuss a LNA design solution that can provide gain stability over a relatively long time (typically 1000 s). To obtain such a performance, the design needs to cope with temperatures and bias fluctuation dependencies which are the main causes of the gain drift over more than a minute.

2. DIFFERENTIAL AMPLIFIER TOPOLOGY

In this paper, we concentrate on the bipolar technology. Indeed, bipolar transistors provide larger transconductance - thus larger voltage gain - than MOS transistors of the same size and the same biasing and also with better noise and bandwidth performances.[4] Therefore for our embedded applications, the LNA is built using SiGe bipolar transistors from a BiCMOS Application-Specific Integrated Circuit (ASIC) technology. Moreover, the alloy of silicon and germanium (SiGe) in the base of these transistors increases the speed capability of such devices.[5]

Differential pair is an obvious way to be less sensitive to common mode noise by amplifying only differential mode signals: it exhibits high common mode rejection ratio. Moreover, differential pairs are easy to interconnect and cascade (which is needed for high gain requirement). Indeed, they have high common mode input impedance and low differential offset voltage.[6] So, the LNA developed for the X-IFU readout chain is based on a bipolar differential pair.

3. RESISTIVE LOADED DIFFERENTIAL AMPLIFIER

A low noise voltage amplifier can be built using resistively loaded bipolar differential pair (Fig. 2-left). Indeed, in such structure a reasonable voltage gain $|g_m \times R_C|$ of a few dozen is easily obtained. Moreover, the total

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input voltage noise density* can be predicted following the equation 1, with k_B the Boltzmann constant, T the temperature in Kelvin, $R_{BB'}$ the parasitic access resistance to the base active region of the bipolar transistor, q the electron charge in absolute value, I_B the base current, R_S the output impedance of the previous stage (SQUID array), h_{11} the differential input impedance† of the bipolar transistor, I_C the collector current (half of the current bias I_{BIAS}), g_m the transconductance of the bipolar transistor and R_L the load resistance. A factor of $\sqrt{2}$ is due to the same independent contributions of the two bipolar transistors. Regarding the 1-6 MHz frequency range considered for the X-IFU readout chain, Flicker noise is not considered in the equation 1 assuming that 1/f noise appears only at lower frequency. Simulations discussed later (Fig. 2 and 3 right) show that the 1/f noise corner frequency is about 1 kHz.

$$\sqrt{S_v} = \sqrt{2} \times \sqrt{4k_BTR_{BB'} + 2qI_B \times \left(\frac{(R_{BB'}+R_S)h_{11}}{R_{BB'}+R_S+h_{11}}\right)^2 + \frac{2qI_C}{g_m^2} + \frac{4k_BT/R_L}{g_m^2}} \tag{1}$$

If care is taken to choose: a sufficiently large transistor size to reduce the $R_{BB'}$, a source resistance R_S smaller than h_{11} (standard requirement for a voltage amplifier) and a load resistance R_L large enough (usually the case in order to provide large voltage gain), the input voltage noise density could be simplified as equation 2. Thus, it remains only fundamental Shot noise: fluctuation in the number of carriers - electrons - crossing a junction and expressed as $\sqrt{2qI}$ in termes of current noise density, with I the junction DC bias current. Equation 2 shows both contributions of the equivalent input current and voltage noise sources, i_n and e_n respectively. i_n is caused by the input Shot noise $\sqrt{2qI_B}$ and e_n by the output Shot noise $\sqrt{2qI_C}$.

$$\sqrt{S_v} = \sqrt{2} \times \sqrt{\underbrace{2qI_B}_{i_n^2} R_S^2 + \underbrace{2qI_C/g_m^2}_{e_n^2}} = \sqrt{2} \times \sqrt{2q\frac{I_C}{\beta}R_S^2 + 2qI_C/\left(\frac{qI_C}{k_BT}\right)^2} = \sqrt{2} \times \sqrt{2q\frac{I_C}{\beta}R_S^2 + \frac{2(k_BT)^2}{qI_C}} \tag{2}$$

In this last expression, the base current I_B can be replaced by I_C/β and the transconductance by the expression $\frac{qI_C}{k_BT}$. Thereby, a minimum input voltage noise is reached for an optimum collector current $I_{C_{opt}}$ given by equation 3. Taking into account a non-zero source resistance R_S, the optimum input noise is reached when $i_nR_S = e_n$ (Eq. 3). It is usual to determine the optimum resistance $R_{S_{opt}}$ for a given commercial LNA.[7] From a LNA designer point of view, we determined the optimum current $I_{C_{opt}}$ for a given R_S specified by other constraints.

$$i_nR_S = e_n \quad \rightarrow \quad 2q\frac{I_{C_{opt}}}{\beta}R_S^2 = \frac{2(k_BT)^2}{qI_{C_{opt}}} \quad \rightarrow \quad I_{C_{opt}} = \frac{k_BT}{q} \times \frac{\sqrt{\beta}}{R_S} \tag{3}$$

Using an AMS 350 nm SiGe BiCMOS technology, the maximum current gain β is about equal to 230. The current status of the X-IFU instrument gives us an output impedance of the SQUID array stage $R_S \approx 200$ Ω. These numerical values lead to a typical optimum collector current I_C close to 2 mA. So we chose for the differential pair a $I_{BIAS} = 4$ mA. This low noise design of the amplifier allows us to reach a voltage input noise smaller than 1 nV/$\sqrt{Hz}$ taking into account all the noise contributions (Fig. 2-right).

The voltage gain follows roughly the equation 4. The load resistance can thus be tuned to adjust the gain; keeping R_L value of the order of a few hundred ohms for output common mode reasons. So, with $g_m = \frac{qI_C}{k_BT} \approx$ 77 mS the voltage gain is roughly equal to 24 with $R_L = 370$ Ω and taking into account the small attenuation due to the 200 Ω source resistance‡ and the output buffer added for lowering the output impedance.

$$|Gain_R| = g_m \times R_L = \frac{qI_C}{k_BT} \times R_L \qquad \propto \frac{I_C}{T} \tag{4}$$

*$\sqrt{S_v}$ is an Amplitude Spectrum Density (ASD) in term of voltage; given in [V/$\sqrt{Hz}$]. It takes into account both contribution, equivalent input voltage noise source e_n and input curent noise contribution into a source resistance $i_n \times R_S$.

†$h_{11} = \beta/g_m$ with β the transistor current gain and $g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{k_BT}$ the transconductance.

‡The input impedance of the amplifier is in first approximation $2\times h_{11} = 2\times\beta/g_m \approx 5$ $k\Omega$

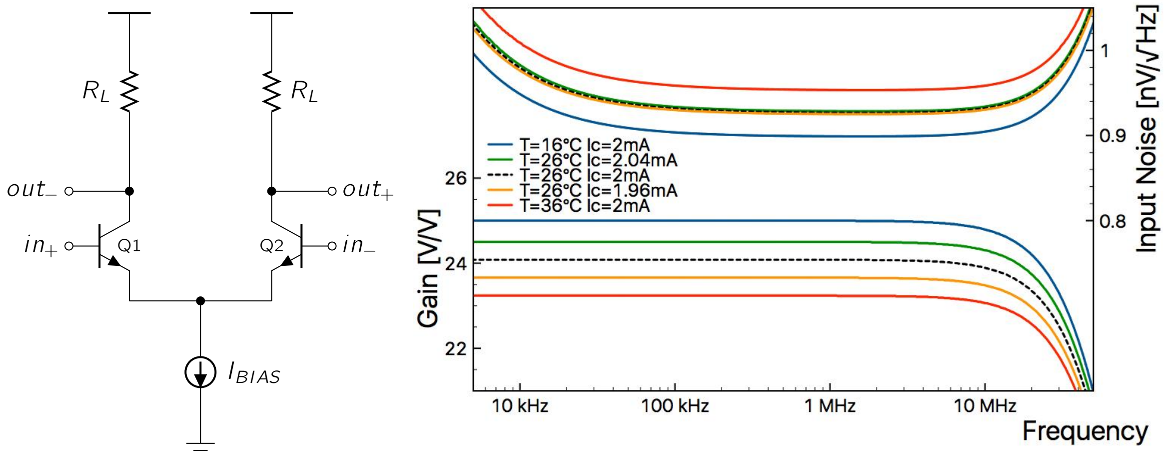

Figure 2. (left) Simplified schematic of the front-end of a low noise amplifier using a resistive loaded bipolar differential pair. (right) Cadence simulations showing the fluctuation of the gain and the noise as function of T and $I_C = I_{BIAS}/2$. A source resistance $R_S = 200\ \Omega$ and emitter follower buffers are added to the resistive loaded differential pair for a realistic gain and noise simulations.

However, the gain (equation 4) is directly proportional to the bias current value and to the inverse of the temperature. For long durations, a fluctuation of the temperature or of the bias directly impacts the voltage gain value. In the case of the X-IFU, with the requirement for a voltage gain drift smaller than 10^{-4} over dozen minutes or more, this amplifier topology is not permitted.

4. DIODE LOADED DIFFERENTIAL AMPLIFIER

Figure 3-left shows again a differential pair topology. We only have replaced the resistive load by diodes. Indeed, diode small signal impedance $r_d = \frac{k_B T}{q I_C}$ has exactly the same expression as the inverse of the bipolar transistor transconductance. Therefore, the voltage gain of such diode loaded differential pair amplifier can be expressed as equation 5, with n_D the number of diodes in series used as load. The larger the number of diodes there is, the larger the voltage gain will be.

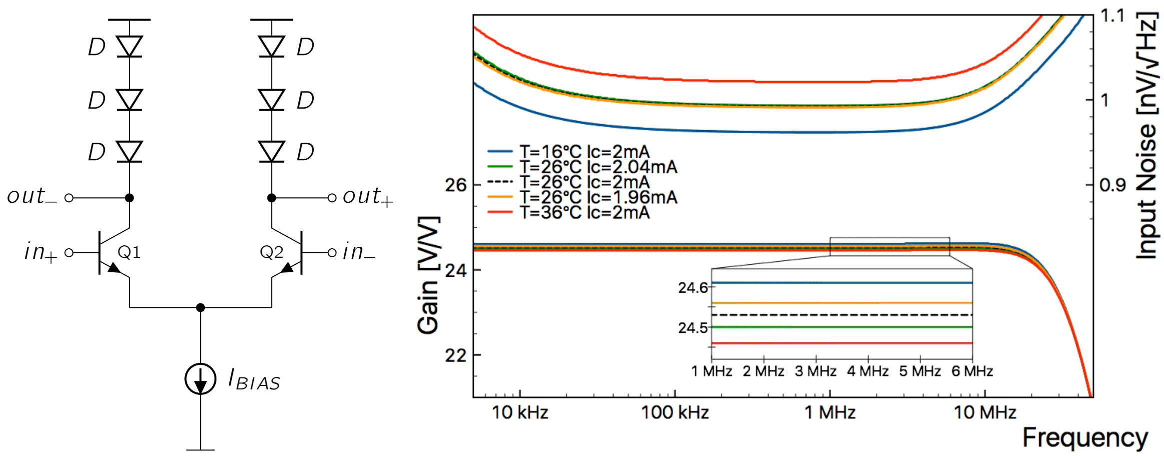

Figure 3. (left) Simplified schematic of the front-end of a low noise amplifier using a diode loaded bipolar differential pair. (right) Fluctuation gain and noise as function of T and I_C simulated for 3 stages of diode loaded differential pair with a source resistance $R_S = 200\ \Omega$.

$$|Gain_D| = g_m \times n_D \times \frac{k_B T}{q I_C} = n_D \qquad \forall\ I_C \text{ and } T \tag{5}$$

In such amplifier, the voltage gain is only determined by the number of diodes; dependancies in temperature and in biasing are compensated. **Gain is virtually independent of the temperature and of the current bias**. Figure 3-right shows gain and noise simulations performed on 3 amplifier stages each loaded by 3 diodes leading to a total voltage gain of 24.5 V/V[§].

Due to the voltage bias usually limited to a few volts[¶], and knowing that a diode introduces a typical 0.6-0.7 V threshold, only a few diodes can be placed in series, limiting the voltage gain of this topology to 2 or 3. Nevertheless, this wide-band[‖] amplifier can easily be cascaded. Moreover, this topology provides a low output impedance not requiring output buffer, at the opposite of the resistive loaded amplifier. The differential output impedance of a diode loaded differential pair is roughly 2 times the impedance of the diodes $n_D k_B T/(q I_C)$. With 3 diodes and 2 mA in the collector, the differential output impedance is smaller than 100 Ω with no buffer.

Regarding the noise, equation 6 gives a simplified expression of the input voltage noise that we can compare with equation 2 obtained for resistive loaded amplifier.

$$e_n = \sqrt{2} \times \sqrt{2qI_B R_S^2 + \underbrace{\frac{2qI_C}{g_m^2}}_{\text{output transistor shot noise}} + \underbrace{\frac{2qI_C}{3g_m^2}}_{\text{diodes shot noise}}} = \sqrt{2} \times \sqrt{\underbrace{2q\frac{I_C}{\beta}}_{i_n^2} R_S^2 + \underbrace{\frac{4}{3} \times \frac{2(k_B T)^2}{qI_C}}_{e_n^2}} \tag{6}$$

Equation 6 shows that the price we pay to stabilize the gain is only an increase of the output shot noise by a factor of 4/3 due to the diode contribution. Output Shot noise is only an half of the total noise (optimum I_C). Therefore, with the same 2 mA collector current used for the resistive loaded amplifier, the simulated input voltage noise density is kept just below 1 $nV/\sqrt{Hz}$ as shown in figures 3.

5. DISCUSSION

Simulations have shown that comparing with resistive loaded amplifier (Fig. 2), the gain fluctuation of the diode loaded differential pairs (Fig. 3) is reduced by an order of magnitude which gives us the temperature range required for the WFEE in the X-IFU instrument. Indeed, with this diode loaded topology, the temperature should not fluctuate more than 0.1 % to satisfy a minimum 10^{-4} required gain stability. This corresponds to a maximum temperature range of 0.3° at room temperature, 10 times larger than what would have been needed if a resistive loaded topology had been used. This relaxes the thermal constraints on the WFEE stage even if thermal regulation in the range of 0.1° is again needed.

A low noise amplifier using the discussed *diode loaded* topology has been realized in BiCMOS SiGe 350 nm technology. This prototype is currently manufactured and soon will be under test in order to measure its ability to compensate the fluctuations of biasing and temperature. Moreover, radiation tests will be performed to qualify such an amplifier for space applications which is needed for the Athena mission.

[§]3 diodes lead to a voltage gain of 3 V/V; 3 stages perform a $3 \times 3 \times 3 = 27$ V/V; source impedance (SQUID array) of 200 Ω, differential input impedance of the amplifier $2 \times h_{11} \approx 5$ kΩ and 3 stages slightly reduce this total gain to 24.5 V/V.

[¶]The 350 nm BiCMOS SiGe technology referred is specified for a 3.3 V power supply.

[‖]Assuming a fairly constant Gain-Banwidth product.

6. CONCLUSION

Fixing the gain can be done by the use of a feedback. However, resistive feedback at room temperature inevitably increases the noise to an unacceptable level for our low noise X-IFU readout chain. Indeed, in such case Johnson noise of the resistors used in the feedback exceeds the other noise contributions. In addition, the LNA discussed in this paper must already be used in a feedback loop: the base-band feedback of the frequency SQUID domain multiplexer (Fig. 1). Therefore using a feedback in the LNA is like putting a loop within a loop, which can mix and complicate the whole chain stability conditions. Diode loaded differential pair is a simple and robust solution for LNA design that, with no-feedback-loop, stabilizing the gain over a long duration, when temperature and biasing fluctuations usually dominate.

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REFERENCES

[1] K. Nandra, D. Barret, X. Barcons, A. Fabian, J.-W. den Herder, L. Piro, M. Watson, and the Athena team collaboration, "Athena - the advanced telescope for high energy astrophysics - a mission addressing the hot and energetic universe science theme," 2015.

[2] L. Gottardi, H. Akamatsu, M. P. Bruijn, R. den Hartog, J.-W. den Herder, B. Jackson, M. Kiviranta, J. van der Kuur, and H. van Weers, "Development of the superconducting detectors and read-out for the X-IFU instrument on board of the X-ray observatory ATHENA," *Instrumentation and Methods for Astrophysics (astro-ph.IM)* , 2016.

[3] L. Ravera, C. Cara, M. T. Ceballos, X. Barcons, and D. B. et al., "The DRE: the digital readout electronics for ATHENA X-IFU," in *Space Telescopes and Instrumentation 2014: Ultraviolet to Gamma Ray*, *Proc. SPIE* **9144**, 2014.

[4] A. Alvarez, *BiCMOS Technology and Applications*, Springer Science & Business Media, 1993.

[5] J. Cressler and G. Niu, *Silicon-Germanium Heterojunction Bipolar Transistors*, Artech House, Boston, MA, 2003.

[6] P. Allen, *Analog Integrated Circuits and Systems - BJT Differential Amplifier*, ECE 4430, 2000.

[7] G. Brisebois, "Op amp selection guide for optimum noise performance," tech. rep., Linear Technology.