Conceptual design of the X-IFU Instrument Control Unit on board the ESA Athena mission

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ABSTRACT

Athena is one of L-class missions selected in the ESA Cosmic Vision 2015-2025 program for the science theme of the Hot and Energetic Universe.

The Athena model payload includes the X-ray Integral Field Unit (X-IFU), an advanced actively shielded X-ray microcalorimeter spectrometer for high spectral resolution imaging, utilizing cooled Transition Edge Sensors.

This paper describes the preliminary architecture of Instrument Control Unit (ICU), which is aimed at operating all X-IFU's subsystems, as well as at implementing the main functional interfaces of the instrument with the S/C control unit. The ICU functions include the TC/TM management with S/C, science data formatting and transmission to S/C Mass Memory, housekeeping data handling, time distribution for synchronous operations and the management of the X-IFU components (i.e. CryoCoolers, Filter Wheel, Detector Readout Electronics Event Processor, Power Distribution Unit).

ICU functions baseline implementation for the phase-A study foresees the usage of standard and Space-qualified components from the heritage of past and current space missions (e.g. Gaia, Euclid), which currently encompasses Leon2/Leon3 based CPU board and standard Space-qualified interfaces for the exchange commands and data between ICU and X-IFU subsystems.

Alternative architecture, arranged around a powerful PowerPC-based CPU, is also briefly presented, with the aim of endowing the system with enhanced hardware resources and processing power capability, for the handling of control and science data processing tasks not defined yet at this stage of the mission study.

Keywords: space telescope, astronomical instrumentation, X-ray spectrometer, control electronics

1. INTRODUCTION

Athena[1][3] has been selected by ESA as the L2 mission (due for launch in 2028), to address the "Hot and Energetic Universe" science theme. The Hot and Energetic Universe refers to the baryonic component of the Universe at such high temperatures, which is largely undetectable by observational facilities at wavelengths longer than X-rays.

About half of the baryonic content in the Universe is expected to be at T > 10^5 K, and there are as many baryons at T > 10^7 K trapped in galaxy clusters as there are locked into stars. There is an intimate relation between this hot gas, which delineates the large-scale structure of the Universe, and the most energetic phenomena occurring in the immediate vicinity of super-massive black holes, through a poorly known process called Cosmic Feedback. The intimate link between the hot and the energetic Universe calls for an X-ray observatory class mission to study these and other related topics.

To address the above topics, as well as many other fundamental questions in contemporary astrophysics, Athena is conceived as a single large-aperture X-ray observatory equipped with two focal plane instruments: a Wide Field Imager (WFI) providing sensitive X-ray imaging over a large field of view, and an X-ray Integral Field Unit (X-IFU) delivering spatially resolved high-resolution X-ray spectroscopy.

The WFI[2] is Si-based detector with DEPFET active pixel sensor readout, delivering sensitive imaging capabilities over a large field of view, modest energy resolution and high count-rate capability. The X-IFU[4] is a calorimeter array, whose front-end sensor is made of absorbers thermally coupled to Transition Edge Sensors operating at 50 mK. It will provide spatially resolved high-resolution X-ray spectroscopy for both point-like and extended sources.

In the following sections, we discuss the X-IFU architecture, section 2, along with its functional and control needs the

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Instrument Control Unit (ICU) has to manage. In section 3, the preliminary architecture is described in the light of the current definition of control interfaces of the X-IFU subsystems, in the aim at showing the maturity, in terms of Space qualification, of the proposed HW configurations and adopted hardware solutions.

2. THE X-IFU BASELINE CONFIGURATION

The X-IFU functional diagram is depicted in Figure 1, and is briefly described hereafter. The X-IFU detection principle is based on an array of X-ray absorbers connected to Transition Edge Sensors (TES), acting as a micro-calorimeter. The TES senses the heat pulses generated by X-ray photons when they are absorbed and thermalized. The temperature variation - a 300-400 microsecond pulse, characterized by sharp increase followed by a slower decay - is measured by the change in the electrical resistance of the TES, which must be cooled to temperatures less than 100 mK (the thermal bath is at 50 mK), and biased in its transition between super conducting and normal states.

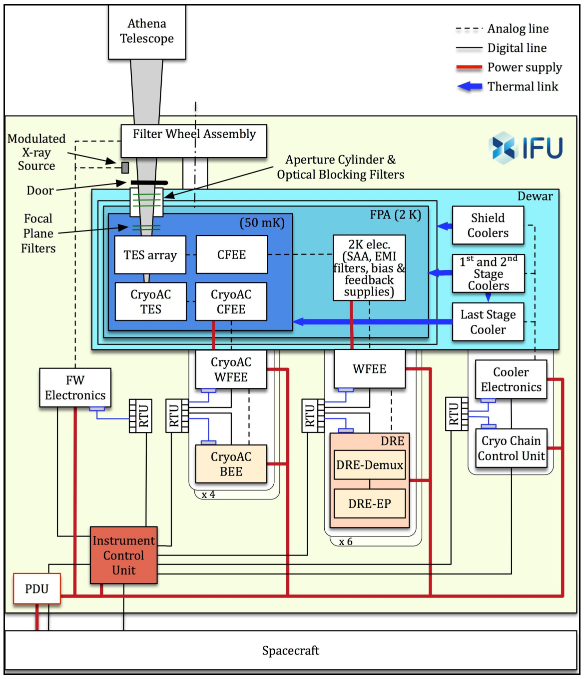

Figure 1 Block diagram of the current X-IFU baseline configuration with main system components and the two stages - 50mK and 2K - cryo-cooler.

The small current of the TES is read out using a low noise amplifier chain consisting of a superconducting quantum interference device (SQUID) in the cold front-end electronics (CFEE) at 50mK, SQUID array amplifiers at 2 K and a semi-conductor low-noise amplifier in the warm front-end electronics (WFEE).

Frequency Domain Multiplexing (FDM) is used to reduce the number of readout channels and hence the thermal load on the cooling chain: a single modulated AC signal biases a group of pixels, with each frequency component matching the resonant frequency of a LC circuit of each individual pixel. The frequency-modulated current of the pixels group is sensed by a single SQUID; successive de-modulation of the SQUID signal enables the reconstruction of the shape of the signal in each pixel. The adoption of a 5 MHz signal bandwidth and a 100 KHz carrier separation allow multiplexing of up to 40 pixels in a single readout channel.

The coverage of the X-IFU field of view, 5’ in size in the current design, requires 3840 equal size pixels; which need up to 96 readout channels of 40 pixels each.

X-IFU cooling chain is designed as a combination of passive radiator, 15 K pulse tube coolers, 2 K Joule Thomson loops and a 50/300 mK hybrid cooler.

The warm Digital Readout Electronics (DRE)[5] takes care of the full control of the acquisition chain, and it is conceived as three functional units:

- DRE-DEMUX is a multi-boards unit to manage TES voltage biases, multiplexing and de-multiplexing of the sensor signals, and pixel signal digitization;
- TRIGGER module performs preliminary event detection and triggering by dedicate FPGA-based boards;
- DRE Event Processor (DRE-EP) is for successive refined signal pulse analysis for X-ray event recognition likely to be accomplished in SW by dedicated CPU-based boards.

The on-board data processing allows reducing significantly the science output data rate, so as to be compliant with the telemetry rate constraints of the mission.

The DRE configuration is still under definition and architecture optimization is ongoing to trade-off system mass, complexity, power consumption, power processing, telemetry data rate and functional redundancy.

DRE baseline foresees from 4 to 6 identical, parallel acquisition chains, including demux board, event trigger board and processor board, and the processor board proving nominal and redundant interfaces both TM/TC handling and for science data packet transfer. Architectural option contemplates to convey data from 4 or 6 DEMUX boards to a redundant processing chain, i.e. Nominal plus Redundant units with event trigger board plus processor board each.

Located closely underneath the TES array, an active anticoincidence layer (Cryo-AC) screens the high energy particle background. In the current baseline, the Cryo-AC detection chain[8] consists of 2x2 pixels TES array (covering the area of interest larger than the X-IFU science detectors), the associated cryogenic SQUIDs and related warm control electronics.

The anticoincidence detectors are controlled individually in DC-mode (i.e. no frequency multiplexing) by the Cryo-AC electronics (CryoAC WFEE); the sensed pulse signals from Cryo-AC WFEE feed the warm back end electronic (Cryo-AC-WBEE) module for signal digitization and pre-processing. Both Cryo-AC WFFE and WBEE modules include nominal and redundant sections.

The filter wheel assembly (FWA), outside the cryostat, is required to reduce the signal load on the detector when observing bright sources and to keep the count rate in the X-rays at acceptable level so as to preventing degradation of the energy resolution. Besides closed position and filters, FWA can also possibly hosts electrically controlled calibration sources are also required to correct for gain drifts in the detectors; although, the exact location of the calibration source is still under definition.

FWA is operated by the Filter Wheel Electronics (FWE) in redundant configuration, using the provided commanding and telemetry interface.

The Instrument Control Unit (ICU) is responsible for operating the instrument with the desired settings, and collects system housekeeping and science data to be transferred to the S/C Mass Memory (MM); the ICU preliminary design is describe the following section.

The power distribution unit (PDU) produces, from the satellite unregulated primary power, the raw power to the different electronic units of the instrument by dedicated supply modules, so as to power each X-IFU independently; the satellite control system manages ICU's power line via dedicated High Priority Command; while, the power distributions to other X-IFU modules is under the control of ICU, which handles the PDU by the instrument's commanding and telemetry link.

3. X-IFU ICU CONCEPTUAL DESIGN

The X- IFU ICU is in charge of the overall control of the instrument, and has to implement telemetry/command and science data interfaces with all the other of X-IFU electronics modules – including DRE-WFEE, Cryo-AC electronics (CryoAC-BFEE and CryoAC-WFEE), FWE, Thermal Control Unit, Cryo Chain Control Unit, PDU - and with the Spacecraft (S/C).

The operational context of ICU within X-IFU is schematically shown in Figure 2, which gives a high level view of the communication interfaces (I/Fs) and of the redundancy concept to implement.

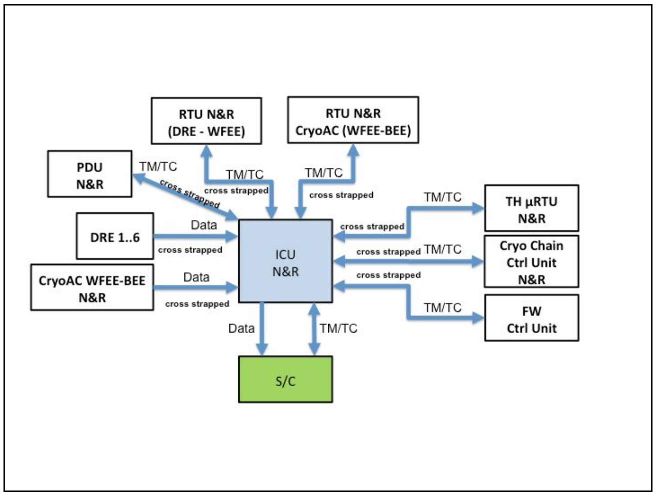

Figure 2 X-IFU ICU operational context with fully redundant electronics in cross-strapped interconnections

X-IFU redundancy concept relies on electronics modules with nominal and redundant sections, and I/Fs to be handled in cross-strapped mode, which improves the reliability figure of the instrument but increases the complexity of the system and the of interconnecting harness.

Within such redundancy framework, the ICU has to manage the following functionalities:

- Telemetry and Telecommand (TM/TC) exchange with the S/C
- Instrument Commanding, based on the received and interpreted Telecommands
- Instrument monitoring and control, based on the Housekeeping data acquired from the instrument units
- Data acquisition from detectors front-end electronics, compression and formatting according to the Telemetry protocol
- Synchronization of all the instrument activities

The ICU functions will be implemented in the On Board Software, which will demand realtime and multitasking execution environment; the selection of the operating system (OS) will depend on the processor technology adopted.

The required SW and HW functions, along the other system constraints - encompassing mass and power budgets, data rate and redundancy – call for a well optimized and compact HW architecture, possibly also featuring enough computational power to afford on board data compression prior the data transfer to satellite mass memory.

3.1 Cross-strapping Implementation

From the HW point of view, the implementation of the ICU functions has to take also into account the expected data rates from X-IFU electronics, which drive the selection of the physical layer for the communication I/Fs among the available standard, space-qualified solutions as MIL-STD 1553, SpaceWire (SpW) or serial, high-speed, multi-drop links like EIA STD RS-485.

Current evaluations assume the following data throughputs:

- DRE's science data links bit rate should not exceed 2.5 Mbps (worst science case - e.g. Crab source - and assuming conservative 30% of events processed by the DRE processing chain), compatible with the operational bandwidths of the SpaceWire (~ 100 MHz) and RS485 (~ 5MHz);
- Cryo-AC's data link is quoted for order of few 100 Kbps, which can be allocated with enough margin within the sustainable rate of 1MHz of 1553 bus, and with increased margin in the 5 MHz bandwidth of RS-485;
- The burden of Telemetry and Command links among ICU, the other X-IFU subsystems and S/C is expected quite modest in the range of few10 Kbps, i.e. as typical telemetry rate from instrumentation operated in Space.

According to these preliminary figures, the RS-485 medium results a good candidate for the implementation of both science data links and of TM/TC links as substitute of the SpaceWire and MIL-1553 bus respectively, which are commonly adopted standards in Space instrumentation.

The RS485 is an LVDS, half duplex multi-point (up 32 devices) and high speed link, and can to greatly simplify the cabling required by the X-IFU cross-strapped if adopted as communal I/F in all instrument units and at S/C level.
Yet, the usage of this physical layer is not so usual as other standards like MIL-1553 bus or SpaceWire; which are fully supported by well defined, developed and proven communication protocols, e.g. Packet Utilization Standard (PUS) services for 1553 bus or Remote Memory Access Protocol (RMAP) for SpaceWire.
Software support and possible reuse already developed software libraries are relevant issues to consider in the choice of physical communication layer.

Driven by the above considerations, two feasible schemes can be proposed, shown in **Figure 3**, for the implementation of X_IFU cross-strapped redundancy.
The first solution (**Figure 3**, left pane) employs a RS485 bus as high-speed data link for the transfer of preprocessed events from DRE and Cryo-AC electronics to ICU. Two additional RS485 bus are proposed as telemetry and commanding link: ICU manages as RS485 master the internal X_IFU TM/TC link to control other X_IFU electronics modules; the second RS485 bus is used by the S/C to command the instrument and to receive telemetry.
ICU assemblies are also endowed with SpaceWire ports for the transfer of compressed X-ray event data packets to the S/C mass memory.
In such configuration, cross–strapping can be easily achieved by the usage of nominal and redundant RS485 bus.

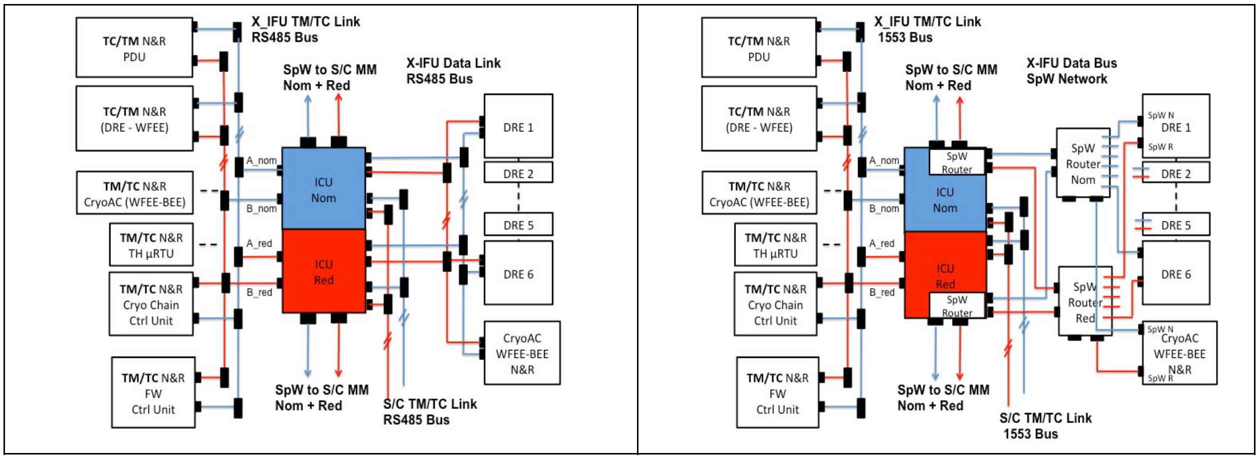

Figure 3 Possible Cross-Strapped Schemes for X-IFU Interconnections: left) Optimized cabling with RS485 buses used for intra instrument and S/C TM/TC links, and for the event data transfer based on multi-point RS485, SpaceWire (SpW) channels for science data transfer to S/C Mass Memory (MM); right) Fully Space-qualified and proven option based on 1553 bus for TM/TC handling and on SpW networks for the science data transfer, selected as baseline solution for the ICU design. It assumes to have SpW routers embedded in the DRE assembly, with the aim of reducing the complexity of the cabling of instrument SpW network.

In the alternative configuration (**Figure 3**, right pane), only common Space standard links are implemented. Telemetry and commands channels use the dual, intrinsically redundant MIL-553 bus for both intra-instrument communication and with the S/C. SpaceWire standard is used for all data links. The internal X-IFU data bus between ICU assemblies and detectors electronics is conceived as SpaceWire network based on redundant SpaceWire Routers.
Cross strapping cabling of the SpaceWire network (based on point to point links) can be achieved with acceptable complexity using a proper distribution of SpaceWire routers between ICU assembly and detector front-end electronics.
The most attractive option is to embed, in the DRE, redundant SpW routers, which link DRE processor chains and Cryo-AC outputs to ICU routers. This allows reducing the number of long cables expected between ICU and front-end electronics, keeping the large number of short connections at the level of front-end units.
The needed modification of the DRE configuration will be assessed with X-IFU system team; a preliminary scheme is shown in **Figure 4** for the case implementing six parallel processing chains.

By the current study phase, the latter approach, utilizing HW and SW well-supported Space standards, is adopted as reference scheme for the design of the ICU.

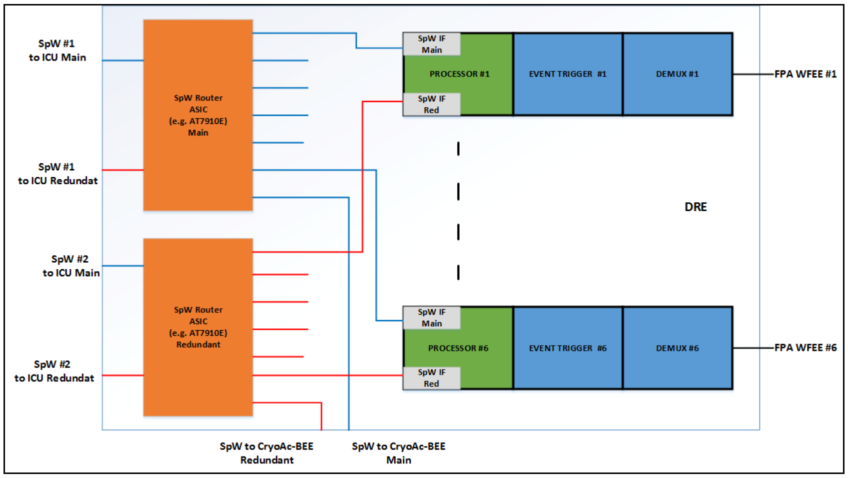

Figure 4 Concept for SpaceWire routing in DRE unit aimed at simplifying intra instrument cabling of the SpaceWire network for cross-strapping implementation

3.2 ICU Preliminary Design

In the current study phase of mission, the design of all X-IU electronics units are in a very early development stage and the definition of the communication interfaces of X-IFU's subsystems is still on going and not finalized yet.
This imposes to approach the ICU design by an adaptable architecture, easily reconfigurable to meet the needs emerging during the design consolidation. The ICU concept is aimed also at exploiting heritage and expertise from launched (e.g. Planck) and under development (e.g. Euclid)[6][7] Space missions.
Reliability and radiation hardening are also common features Space electronics have to provide.

The architectural concept of X-IFU's ICU relies on the following basic assumptions:

- all X-IFU's subsystems are intelligent units capable of autonomous control of connected devices without the intervention of the ICU;

-all X-IFU subsystem are connected in cross-strapping redundancy;

- ICU has to coordinate the activities by dispatching commands received from the S/C, and to monitor the status of the instrument by the collected housekeeping;

- ICU is not charged of any processing task on science data, with the exception of data compression, if needed, before the transfer to satellite mass memory.

The basic configuration of X-IFU's ICU is conceived as two identical sections in cold redundancy, i.e. only one section is operating at a given time.
Each section will host likely three boards: a power supply board (DC/DC converters), a CPU–based controller board executing the On Board Software, and a Data Router Board (DRB) for science data and system HK management.
Given the limited number boards, the two sections can be arranged in the same box.

Individually, sections can manage the full instrument and are equipped with two MILBUS 1553 interfaces: one acts as Remote Terminal (RT) and exchange TC/TM with S/C; the second implements the Bus Controller (BC) function for commanding and telemetry handling internally X-IFU.
High rate data transfer is supported by SpaceWire interfaces: one is to receive science data from DRE and another towards the S/C is used for the transfer of compressed data to satellite Mass Memory; both SpW interfaces are implemented with two links for enabling cross-trapped redundancy.
Substitutes for MIL-1553 and SpaceWires, like high-speed serial link based on RS485 technology, will be considered as an option, to be studied as trade-off.

Specific system features – internal system bus, functions and I/Fs of Data Router Board (DRB) – depend on the CPU technology of the controller board, whose choice is also driven by the implementation of the on board data compression.

In the current study phase of the program, two design options are considered, shown in **Figure 5**:
- ICU baseline solution is designed around a LEON2/3 Fault Tolerant (FT) processor, and the data compression is performed in HW by a dedicated FPGA or ASIC.
- The backup solution considers the usage of Power-PC CPU with enhanced processing power capability to control the instrument and to perform data compression by software.

3.2.1 Leon-based baseline solution

Leon is 32-bit processor compliant with the SPARC V8 architecture, which makes use of AMBA Advanced High-speed Bus (AHB) and Advanced Peripheral Bus (APB), interfacing high-bandwidth units and low speed peripherals. The architecture is particularly suitable for implementation on radiation tolerant FPGAs and for system-on-a-chip (SoC) designs.
Leon microprocessors are available in different synthesizable VHDL models, including advanced fault-tolerance features that make them particularly suited for embedded systems in Space applications.
The variant Leon2-FT (Fault Tolerant) is available in framework of ESA programs as VHDL IP Core along with a library of others VHDL IP Cores of modules (e.g. EDAC controller) and peripherals (e.g. SpaceWire and MIL-1553) for the implementation of a custom system on radiation tolerant FPGAs or as a rad-hard SoC in ASIC.
The Leon3-FT variant is an extension of Leon2 processor, allowing multi multiprocessing configuration with up to 16 CPUs. Leon3 is an Aeroflex Gaisler development, and in the single core SoC version is implemented in RTAX2000S FPGA.
Software development for Leon family processors is supported by real time executive environment RTEMS.
Leon2/3-FT processors are TRL9 solutions; they currently run flight computers on board of ESA's missions (e.g. Proba-2, Venus Express).

Synthesizable approach based on FPGA enables easy hardware changes during the design and development phases, so as to adapt the system to the specific application's needs and according to the consolidation of functional requirements: e.g. peripherals and interfaces - like SpaceWire links, PCI interface, MIL-1553 or UART - can be included design by instantiating the corresponding IP cores onto the AHB or APB bus.

In the baseline option, the CPU board is a typical Leon unit (**Figure 5**, left pane) with two 1553 I/Fs for BC and RT functions. The AMBA AHB bus is routed through the unit backplane and is also used as main IF with Data Router Board.
DRB functions include:
- data compression in HW, implemented by a custom RTAX FPGA or using the CWICOM ASIC developed by EADS ASTRIUM in the framework of ESA activities; for the being, the latter is assumed for the concept shown in **Figure 5**.
- SpaceWire Router to handle the transfer of science data between DRB and X-IFU electronics and S/C mass memory units.
- Data buffering for temporary storage of transiting detector data.
- Clock and Synchronism generator, that provides clocks for DRB elements and reference time signals to be delivered to X-IFU detectors electronics for accurate event triggering.
- Interface Logic by a dedicated radiation tolerant FPGA, which links DRB modules and makes available DRB functions to CPU board through the AMBA AHB I/F.

3.2.2 Power-PC based option

The proposed ICU backup configuration (**Figure 5**, right pane) is designed around the Power-PC SCS750 board developed by Maxwell Technologies INC, which is currently in use in Gaia and it has been also adopted for the data processing units of the two instruments, NISP[7] and VIS, of the Euclid mission. The Maxwell SCS750 is also a flight proven TRL9 solution.
The Power PC Module contains three IBM PowerPC® 750FX processors, which are configured in Triple Module Redundancy (TMR). It is capable of processing at up to 1800 MIPS and is supported by 8MB of EEPROM and 256MB of SDRAM EDAC protected. The Power PC Module provides General Purpose I/O, serial ports for external connections and SW development support, and a redundant MIL-STD-1553B interface.
The SCS750 board is designed to operate in a cPCI system, and is supported by the VxWorks/C real time software environment.

These features - high processing performance, the large amount of SDRAM memory real time operating system- enable to charge the SCS750 application software with instrument control functions, as well as with data processing or data compression, if required.

As a result, the backup solution for the two, nominal and redundant, ICU sections consists of cPCI system still hosting three boards: SCS750 CPU board, the Data Router Board and the power supply DC/DC board.

DRB configuration is slight modified to meet the new system features and to take into the implementation of the data compression function in the application software. The changes with respect the baseline configuration include the removal of the HW data compressor; the adaptation of the interface logic to meet the cPCI specification and to extend the system interface with additional 1553 IF for the Bus Controller function of the internal control bus of X-IFU.

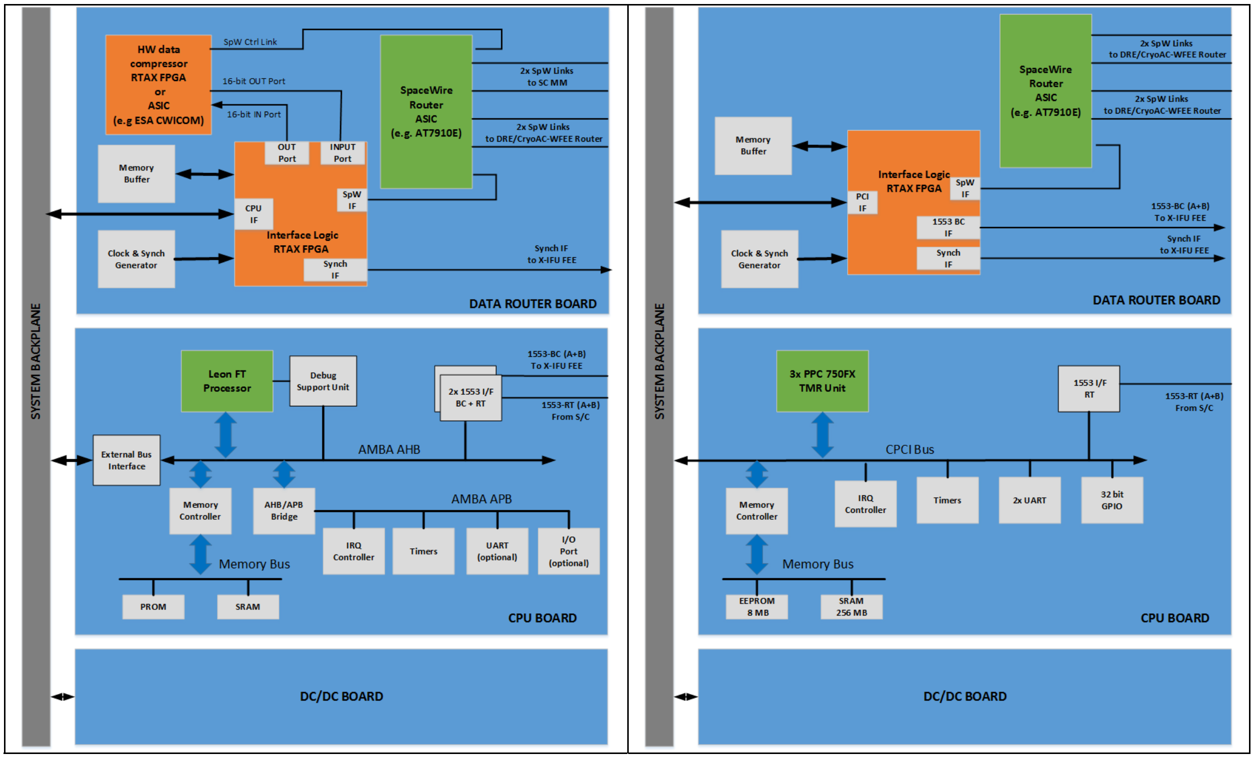

Figure 5 Proposed architectures for X-IFU's ICU: left) Leon-based baseline with compression function implemented in HW by ESA CWICOM ASIC in the Data Router Board; right) Backup option designed around the Maxwell SCS750 board, assuming to provide data compression function by the application software.

4. CONCLUSIONS

Two preliminary concepts of Instrument Control Unit of Athena's X-IFU instrument have been studied with the aim of demonstrating feasibility and maturity of the identified solutions for space application.

Both Leon-based approach, proposed baseline in the current study phase of the mission, and PowerPC-based backup option are conceived as modular unit in which a CPU board and a companion Data Router board are optimized for the implementation of SW and HW functions. Exploiting the heritage of past and current Space science missions, all functions are implemented by using only Space-qualified and fight proven components, as well as Space standard interfaces fully supported for HW and SW development.

The feasibility of X-IFU cross-strapped redundancy has been demonstrated and is supported by the usage of dual, intrinsically redundant MIL-1553 bus for commands and telemetry; science data transfer occurs through a SpaceWire network of acceptable complexity, based on distributed SpaceWire routers between ICU assembly and detectors front-end electronics. Aternative solution based on high speed, serial and multi-drop bus has been also identified.

The ICU modular architecture and the FGPA-based synthesizable approach for the implementation of most functions allow easy hardware changes during the next design or development phases, according to the consolidation of functional requirements of the instrument.

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